IN THE TITLE

Please amend the title as follows:

~~METHOD AND APPARATUS FOR~~ SERIAL BUS TO MULTIPLE JTAG BUS BRIDGE

IN THE SPECIFICATION

[0001] This application is related to copending and cofiled applications for United States Letters Patent Serial No. 09/918,023, filed July 30, 2001 and entitled METHOD AND APPARATUS FOR IN-SYSTEM PROGRAMMING THROUGH A COMMON CONNECTION POINT OF PROGRAMMABLE LOGIC DEVICES ON MULTIPLE CIRCUIT BOARDS OF A SYSTEM (Attorney Docket No. 10016249-1); Serial No. 09/918,030, filed July 30, 2001 and entitled FIRMWARE FOR ACCESSING SCAN CHAINS AND UPDATING EEPROM-RESIDENT FPGA CODE VIA A MANAGEMENT BUS TO JTAG BUS BRDIGE (Attorney Docket No. 10017840-1); Serial No. 09/917,983, filed July 30, 2001 and entitled SYSTEM AND METHOD FOR IN-SYSTEM PROGRAMMING THROUGH AN ON-SYSTEM JTAG BRIDGE OF PROGRAMMABLE LOGIC DEVICES ON MULTIPLE CIRCUIT BOARDS OF A (Attorney Docket No. 10016250-1); and Serial No. 09/917,982, filed July 30, 2001 and entitled METHOD FOR JUST-IN-TIME UPDATING OF PROGRAMMING PARTS (Attorney Docket No. 10017845-1)all of the aforementioned applications incorporated herewith by reference thereto.

[0004] While the I2C and SPI busses are typically used for communications within systems during normal operation, the IEEE 1149.1 serial bus, known as the Joint Test Action Group (JTAG) bus, was intended for testing of inactive systems by providing access from a tester to perform a boundary scan on each integrated circuit. The tester can thereby verify connectivity of the integrated circuits and verify that they are installed and interconnected correctly. The JTAG bus provides for interconnection of one or more integrated circuits in a chain, any of which may be addressed by the tester. Typically, multiple devices of a circuit board are interconnected into a JTAG chain.

[0022] A particular embodiment is used in a system having multiple boards, where some boards have multiple EEPROMS coupled to provide configuration code to FPGAs. The EEPROM devices of each such board are coupled into a JTAG bus, with a separate bus for each such board. Individual boards may

have multiple JTAG busses. The JTAG chains from each board are routed to the bus bridge. The bus bridge provides an interface between the multiple JTAG busses and one or more processors of the system, as well as selection circuitry such that the processors may address individual JTAG busses of the multiple JTAG busses.

[0039] A particular embodiment of the computer system has sixteen CPUs, another embodiment has four CPUs. Each CPU, such as CPU 236 located on Board F 245, has associated memory 238 and is part of a partition that is capable of running an operating system such as MICROSOFT WINDOWS®, LINUX®, HP-UNIX® or other operating systems as known in the art. The CPUs may be located on a board, such as Board F 245, having an FPGA 239 coupled to receive configuration code from an EEPROM 240, that is in turn coupled to a JTAG bus 246 accessible for programming from common configuration logic 228. CPU 236 is coupled to a network 241, which may incorporate local area networks (LAN), firewalls, and wide area networks (WAN) such as the Internet. Also coupled to the network 241 is a server 242 having an FPGA configuration code database 244.

[0047] The system management subsystem processor 312 then initializes common configuration logic 228, including purging 408 any data remaining in First-In, First-Out, buffers (FIFOs) of the common configuration logic 228, and sets 409 selection register 300 with an identity of the particular JTAG bus coupled to the EEPROMs to be programmed.